ESD Protection Design for Gigahertz Differential LNA in a 65-nm CMOS Process
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Abstract—The electrostatic discharge (ESD) immunity test for EMC was one important reliability regulation. The turn-on-efficient on-chip ESD protection circuit is required to clamp the overvoltage. A novel design of ESD protection diodes with embedded silicon-controlled rectifier (SCR) was proposed to protect the gigahertz differential low-noise amplifier (LNA). Experimental results had shown that the proposed ESD protection design for the differential LNA can achieve excellent ESD robustness and good RF performances.

I. INTRODUCTION
CMOS technologies have been used to implement the radio-frequency (RF) integrated circuits (IC) with the advantages of scaling-down feature size, low power consumption, high integration capability, improving high-frequency characteristics, and low cost for mass production [1]. The IC realized in CMOS technologies are susceptible to electrostatic discharge (ESD) events which may damage the microelectronics products [2]. Therefore, on-chip ESD protection circuits must be added at the RF IC.

The conventional ESD protection design with dual diodes has been generally used for gigahertz LNA [3], as shown in Fig. 1. Under pin1-to-pin2 ESD stresses in the differential LNA, the ESD current will be discharged through D P1, V DD bus, power-rail ESD clamp circuit, V SS bus, and D N2. The pin-to-pin ESD stress was the most critical ESD events for the differential input pads, since the pin-to-pin ESD current path is longer than positive-to-V DD (PD), positive-to-V SS (PS), negative-to-V DD (ND), and negative-to-V SS (NS) ESD current path. In this work, a novel ESD protection design by using ESD protection diodes with embedded SCR for effective ESD protection in the gigahertz differential LNA is presented [4].

II. PROPOSED ESD PROTECTION DESIGN
The new ESD protection design utilizes stacked diodes with embedded SCR, as shown in Fig. 2. This design combines P+/N-well diodes (D P1, D P2, D N1, and D N2) and P-well/N+ diodes (D P3, D P4, D N3, and D N4) to form the embedded P+/N-well/P-well/N+ SCR paths (SCR 3, SCR 4, SCR 5, and SCR 6) by using layout skill. Besides, by putting D P1 and D N4 (D P2 and D N3) together in layout, another embedded SCR1 (SCR2) exists. To implement this design, the layout top view and the device cross-sectional view of the proposed ESD protection design are shown in Figs. 3 and 4.
Fig. 4  Cross-sectional view of novel ESD protection design along (a) A-A’, (b) B-B’, (c) C-C’, and (d) D-D’.

The ESD current paths along A-A’ direction include D_P3, D_P1, D_N4, D_N2, and the parasitic stacked diodes from RF_IN1 to RF_IN2. The ESD current paths along B-B’ direction include SCR_5, SCR_1, and SCR_4. Similarly, the ESD current paths along C-C’ direction include D_N1, D_N3, D_P2, D_P4, and the parasitic stacked diodes from RF_IN2 to RF_IN1, and those along D-D’ direction include SCR_3, SCR_2, and SCR_6.

The width of diode path (T) is equal to twice the width of t in Fig. 3, and the width of SCR path (W) is the sum of all segments of w_1 and w_2. In the beginning of ESD stress, the diode paths will turn on to discharge the initial currents, and then the SCR paths will take over to discharge the primary currents. The diode path also plays the role of trigger circuit of SCR device to enhance its turn-on speed [5]. Since the primary ESD currents are designed to be discharged through the SCR paths, the distance from anode to cathode of SCR (D) is wished to be minimized. The turn-on resistance of SCR can be lowered by using this layout style.

As pin-to-pin ESD stress from RF_IN1 to RF_IN2 (pin1-to-pin2), the ESD current can be discharged by the parasitic stacked diodes with embedded SCR_1. During pin-to-pin ESD stress from RF_IN2 to RF_IN1 (pin2-to-pin1), the ESD current can be discharged by the other parasitic stacked diodes with embedded SCR_2. Comparing with the conventional ESD protection designs, the novel ESD protection design provides the whole chip ESD protection for all ESD-test pin combinations with lowest clamping voltage. Therefore, the novel ESD protection design is expected to have better ESD robustness.

III. APPLICATION OF NOVEL ESD PROTECTION DESIGN TO 24-GHZ DIFFERENTIAL LNA

The differential LNA is designed to operate at 24 GHz with V_DD supply of 1.2 V. The circuit schematic of the reference LNA without ESD protection is shown in Fig. 5. The architecture of common-source inductive degeneration is applied to match the source impedance (50 Ω) at resonance. Using the cascode configuration can achieve good isolation between the input and output. Moreover, cascode configuration reduces the Miller effect and provides good stability.

The LNA with and without ESD protection circuits have been fabricated in a 65-nm CMOS process. The novel ESD protection design with W = 40 μm and T = 10 μm is used to protect the RF_IN1 and RF_IN2 pads of the differential LNA. For comparison purpose, the conventional ESD protection design with the same size (W = 40 μm) is also used to protect the RF_IN1 and RF_IN2 pads of the other test LNA.
IV. EXPERIMENTAL RESULTS

The transmission-line-pulsing (TLP) system is used to measure the I-V characteristics. Fig. 6 shows the TLP-measured I-V curves of ESD protection circuit under pin-to-pin stress.

The RF characteristics are measured on wafer through G-S-G-S-G microwave probes. Each LNA operates with the 1.2-V $V_{DD}$ supply and draws a total current of 18 mA. The used bias voltage driven through the external bias tee is 0.65 V. The RF performances of all LNA are measured before and after ESD stress. The measured $|S_{21}|$ parameters of all LNA are shown in Figs. 7–9. The peak gain frequency of the LNA is shifted to about 21 GHz. The shift of the peak gain frequency may be due to the inaccurate device model as frequency higher than 20 GHz, since the device model is only promised below 20 GHz in the given CMOS process. Before ESD stress, the $|S_{21}|$ at 21 GHz of LNA without ESD protection, LNA with conventional ESD protection design, and LNA with novel ESD protection design are 12.3 dB, 11.3 dB, and 11.5 dB, respectively, the $|S_{11}|$ at 21 GHz are all lower than -15 dB.

To verify the ESD protection ability, the RF performances of all LNA after ESD tests are re-measured. All PD, PS, ND, NS, and pin-to-pin modes of HBM ESD stresses are performed to the LNA. The RF performances of the LNA without ESD protection are severely degraded after 0.5-kV HBM ESD tests, as shown in Fig. 7. The RF performances of the LNA with conventional ESD protection design are degraded after 2-kV HBM ESD tests, as shown in Fig. 8. In contrast, the RF performances of the LNA with novel ESD protection design are still excellent matching after 2-kV HBM ESD stress, as shown in Fig. 9.

V. CONCLUSIONS

The novel ESD protection design of diodes with embedded SCR has been developed for the gigahertz differential LNA. Measurement results verify the RF performances and confirm the ESD protection ability of the novel ESD protection design.

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REFERENCES


