A Concurrent Dual-Band 2.4/5.2 GHz Low-Noise Amplifier Using Gain Enhanced Techniques

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Abstract — This paper presents the design and experimental results of a concurrent dual-band 2.4/5.2GHz low-noise amplifier. To achieve the concurrent gain and impedance matching at the both bands, input and output matching using two poles matching and LC resonant network are implementation, respectively. In low-noise amplifier using gain enhanced technique in order to improve gain since LC resonant matching network limit gain. The LNA is has been fabricated in a 0.18-um CMOS process and employs a supply voltage of 1 V. The measured power gain and noise figure for 2.4GHz (5.2GHz) is 12.9dB (8.9dB) and 3.7dB (3.7dB), respectively. The linearity parameters of IP1dB and IIP3 are -14dBm and -4dBm at 2.4GHz, and -11dBm and -1dBm at 5.2GHz, respectively. The power consumption is 7.6mW.

Index Terms—Concurrent, dual-band, low-noise amplifier (LNA), gain-enhanced.

I. INTRODUCTION

In recent years, wireless communications have been rapidly progressing. The implementation of higher speed and longer distance has becoming important on the wireless transmission for human beings. Many communication standards, such as industrial scientific medical (ISM), Bluetooth, wireless local area network (WLAN), etc., are widely used. The increasing demand for wireless services has driven the need for a single communication system to support multi-mode/multi-band signal operation [1].

LNA plays an important role in radio frequency system because it amplifies the signal with contributing small noise to the next stage by introducing inherent noise as low as possible [2]. The LNA determines the frequency range of the entire receive chain, it is necessary to design an LNA that can either receive multiple frequency bands simultaneously or used switch achieve different operated frequency bands [3].

In order to design dual-band LNA, input matching become very important. Many dual-band CMOS LNAs have been developed in literature [4-7]. A straightforward method for operating multiple frequency bands is using switch [4-5]. However switch (MOSFET) method can decrease matching devices reduce chip area, which parasitic capacitor (cgd) with input signal feedback introduces frequency drift in high frequency. The LC resonant matching method introduce concurrent dual-band characters can increase chip area but without signal feedback problem [6-7]. However the LC resonant matching method of the of the output terminal, the maximum gain of the circuit will be limited. To overcome this problem, this work uses a method without increasing too many power consumptions to improve concurrent dual-band low-noise amplifier gain.

In this paper, the circuit design method of proposed concurrent dual-band 2.4/5.2GHz low-noise amplifier using gain enhanced technique presented in sections II. Section III presents the measurement results. Finally, the conclusion is summarized in section IV.

II. CIRCUIT DESIGN METHOD

A. Main Circuit Architecture

Fig. 1 demonstrates the concurrent dual-band LNA using gain enhanced technique. We join a common gate (CG) to common source (CS) in the cascode amplifier to eliminate miller effect and improve isolation.

B. Matching Network

Fig 2(a) shows the input matching network for T matching network and L matching network produce two poles achieve concurrent dual-band. Input impedance can express as eqn. (1).

\[
Z_{in} = \frac{1}{j\omega L_2} + \frac{1}{j\omega L_1} || \frac{Z_m}{j\omega L_2}
\]  

(1)

\[
Z_{in} = j\omega(L_1 + L_2) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_2}{C_{gs}}
\]  

(2)
In order to achieve concurrent dual-band characteristic, we use LC resonant matching in output terminal. The matching method results in both gain limit of maximum and gain attenuation. The gain enhanced techniques adding common gate amplifier \((M_{nt})\) can increase \(g_m\) to improve gain, therefore, gain limit problem could be improved. Fig 3(b) shows gain enhanced techniques, and its architecture can improve trans-conductance \(g_m\) of CG stage amplifier. Therefore, \(g_m\) will improve \((1+A)\) times and can be expressed as eqn. (6) [9]. So, noise factor is decreased because of inverter gain and can be expressed as eqn. (7).

\[
F = 1 + \frac{g_{m2} + \delta g_m}{g_m} = 1 + \gamma \tag{5}
\]

The cascode amplifier with gain enhanced technique is shown in Fig 4. The MOSFET \((M_{nt})\) can increase the output impedance of cascode amplifier. Therefore, the gain can be expressed as eqn. (8) [10].

\[
\left| A_{in} \right|^2 \approx g_{m1} \left( g_{m2} r_o \right) \left( g_{m3} r_o \right) \tag{8}
\]

Fig 4. Schematic circuit of input matching network

III. MEASUREMENT RESULTS

The proposed concurrent dual-band low-noise amplifier is designed with a standard 0.18um 1P6M CMOS technology. The chip size is 0.9x1.0mm² including the pads. This chip was measured by using the method of on-wafer probing. The LNA is operated at frequency of 2.4GHz and 5.2GHz.

Fig 5 showed the stability factor of concurrent dual-band LNA. Fig 6 showed the S parameter measurement result of the S(11). Input return loss is -13.1dB and -10.5dB at 2.4 and 5.2GHz respectively. The gain (S21) of 2.4 and 5.2GHz is 12.92dB and 8.22dB respectively. Input third order intercept point (IIP3) is set at frequency of 2.4 and 5.2GHz. In measurement of IIP3 is -4dBm at 2.4GHz and -1dBm at 5.2GHz as shown in Fig 8(a) and Fig 8(b). Noise Figure of
2.4 and 5.2GHz is 3.7dB and 3.7dB respectively. The current consumption of this concurrent dual-band LNA is 7.6mA with 1V power supply voltage.

Fig. 5. Measurement of Stability Factor

Fig. 6. Measurement of input matching network

Fig. 7. Measurement of gain S(2,1)

Fig. 8(a). Measurement of IIP3 (2.4GHz)

Fig. 8(b). Measurement of IIP3 (5.2GHz)

Fig. 9. Measurement of noise figure
**TABLE I**

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\[
FOM = 20 \log \frac{\text{gain (lin) \cdot IIP3 (mW)}}{p_{dc} (mW) \cdot (NF/\text{lin} - 1)}
\]

**IV. CONCLUSION.**

Fig. 10 showed chip micrograph of dual-band LNA. In conclusion this paper presents a concurrent dual-band low-noise amplifier using gain enhanced techniques based on two poles and LC resonant matching. This process is used in the design of a dual-band LNA that can simultaneously achieve match at 2.4 GHz and 5.2 GHz. This dual-band LNA was fabricated in a 0.18um CMOS process. This LNA has significantly presented features of good noise figure (NF) and outstanding linearity (IIP3) at 2.4 and 5.2GHz.

**REFERENCES**


