Power Integrity Modeling, Measurement and Analysis of Seven-Chip Stack for TSV-based 3D IC Integration

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Abstract—This paper presents power integrity modeling, measurement and analysis of a seven-chip stack for through-silicon via (TSV)-based 3D IC integration. A hybrid full-wave and circuit approach, combined with a cascaded scattering matrix technique, is proposed to model the multi-chip stack consisting of TSVs, on-chip power grids and on-chip decoupling capacitors. The hybrid approach leverages the accuracy of a full-wave approach and shorter computational time of a circuit approach. Modeling results show good correlation with measurement from 1.1 GHz to 20.1 GHz. Power integrity analysis is then performed on the seven-chip stack. To the best of our knowledge, this is the first power integrity modeling, measurement and analysis of seven-chip stack including on-chip decoupling capacitors.

I. INTRODUCTION
Three-dimensional integrated circuits (3D ICs) in the form of chip stacking using through-silicon vias (TSVs) is considered as a key technology in realizing compact and high-performance integrated systems in terms of speed, bandwidth and functionality [1]. However, the increase in the number of on-chip devices due to chip stacking accompanied by the reduction in supply voltage results in higher current in 3D ICs. Furthermore, TSVs and microbumps introduce additional parasitic effects such as inductance to the 3D IC power distribution path. This can potentially lead to larger simultaneous switching noise (SSN) if various stacked chips switch at the same time [2]. Hence, power distribution network (PDN) in 3D ICs need to be accurately modeled and carefully designed.

Due to the complexity of 3D PDN, it is too computationally intensive to model using full-wave approach. Hence, several models for stacked chips were proposed in [2]-[4] based on the equivalent circuit approach. However, those equivalent circuit models of TSVs and on-chip power grids are often simplified without capturing all the relevant parasitic effects as full-wave methods do. Moreover, validation of models with measurements was not reported in those papers. To date, only a few papers reported power integrity analysis of 2 to 3-chip stack based on modeling with experimental verification. In [5], a 2-layer stack consisting of an interposer PDN and an on-chip PDN was modeled by a segmentation method with measurement validation up to 20 GHz. But up to 60% of difference between the modeling and measurement results was reported. In addition, on-chip decoupling capacitors were not included in the model.

In this work, we focus on power integrity modeling and measurement of a 7-chip stack including on-chip power grids, TSVs and on-chip decoupling capacitors. A hybrid full-wave and circuit modeling approach is proposed. It is to leverage the advantages of both the full-wave approach being accurate and the circuit approach being lower memory usage and shorter computational time. The cascaded scattering matrix technique is then used to model the multi-chip stack. The proposed modeling approach is validated against measurement from 1.1 GHz to 20.1 GHz. Based on our modeling approach, frequency-domain power integrity analysis is performed for a single chip as well as the 7-chip stack. The effects of TSVs and vertical natural capacitors (VNCAPs) on the PDN performance are discussed.

II. STRUCTURE OF SEVEN-CHIP STACK
A prototype of a 3D IC system consisting of 6 via-last (VL) chips (12 mm x 12 mm) and 1 via-middle chip (VM) (15 mm x 15 mm) stack assembled on top of a BGA substrate and a PCB has been fabricated (see Fig. 1). The chip process flow can be found in [6]. In this paper, we report on the modeling and measurement results of the single chip and 7-chip stack.

Fig. 2 illustrates the details of the 7-chip stack structure. The 6 VL chips (D2/D3) and 1 VM chip (D1) are stacked face-to-back and the 5 D3 chips contain only TSVs. In each chip, the silicon substrate has a height of 50 µm with a dielectric constant of 11.9 and a conductivity of 10 S/m. A typical ground-signal-ground (GSG) TSV configuration is used and each TSV is made of copper with a conductivity of 5.8x10⁷ S/m. The diameter of the VM and VL TSVs is 8 µm and 40 µm, respectively. In each D1 VM and D2 VL chip, there are 2 layers of alternate power and ground metal lines which form the interleaved on-chip power grid and are
connected through vias. The size of the power grid is 5.6 mm x 1.6 mm and 2.5 mm x 1.5 mm in D1 VM and D2 VL chips, respectively.

Fig. 1 A SEM image of the cross-section of the 7-chip stack on the BGA substrate. Note that TSVs cannot be seen in the cross-section due to an offset between TSVs and microbumps.

There are also 4 layers of VNAPs which are uniformly distributed and connected to the power grid. MOS capacitors are widely used for decoupling solutions. However, leakage current in MOS capacitor increases with technology scaling. Thus, passive VNAP is explored in this paper. VNAP can be fabricated by conventional back-end-of-line (BEOL) technology in CMOS without additional processing steps unlike metal-insulator-metal (MIM) capacitor [7]. Therefore, it attracts increasing attention in high-performance RF integrated circuits. In D1 VM chip, the total number of VNAPs is 156 in each layer and the size of each VNAP is 150 µm by 100 µm. In D2 VL chip, the total number of VNAPs is 15 in each layer and the size of each VNAP is 150 µm by 150 µm.

III. HYBRID FULL-WAVE AND CIRCUIT MODELING APPROACH

To model such a complex chip stack, the following hybrid full-wave and circuit approach (see Fig. 3a) is proposed. Note that this approach can be extended to model a 3D IC system including multi-chip stack, BGA substrate and PCB.

To avoid the computational intensive full-wave simulation of VNAPs, its equivalent circuit model is first extracted from measurement data. Fig. 3b shows a physics-based π-equivalent circuit model of VNAPs [7]. \( R, L, \) and \( C \) represent the metal finger series resistance, series inductance and capacitance between two fingers, respectively. \( C_{ox}, R_{sub} \) and \( C_{sub} \) are the parasitic oxide capacitances between the metal finger and silicon substrate, substrate resistance and substrate capacitance, respectively. The extracted capacitance, \( C \) of the VNAPs in the VM and VL chip is 22.6 pF and 35.2 pF, respectively. These values are close to the measured DC values of the VNAPs.

The extracted VNAP circuit model is then inserted into the model comprising the interleaved on-chip power grid and TSVs to perform full-wave simulation. The resultant scattering matrices of individual chips are then combined together by the cascaded scattering matrix technique [8] to obtain the entire scattering matrix or impedance of the 7-chip stack. This technique has been previously validated against full-wave simulation for the modeling of multi-chip stack comprising a pair of TSVs in each chip [9]. The cascaded method can significantly reduce the simulation time.

IV. POWER INTEGRITY RESULTS, VALIDATION AND ANALYSIS

Power integrity analysis is first performed for each single chip in terms of impedance correlated to measurement. The effects of TSVs and VNAPs on PDN impedance in the single chip are discussed. Next, the PDN impedance of the 7-chip stack is presented correlated to measurement and the effect of chip stacking on PDN impedance is investigated.

A. Single D1 Via-middle and D2 Via-last Chip

A total of 12 ports were designed in D1 VM chip (see Fig. 4) and 9 ports in D2 VL chip (see Fig. 5). GSG TSVs are present at each port location. Note that Ports 3, 6, and 9 of the top D2/D3 VL chip are connected to Ports 10, 12, and 11 of the bottom D1 VL chip through TSVs and microbumps, respectively. On-wafer measurements were performed by using a vector network analyzer (Agilent 8510, bandwidth of instrument: 10 MHz to 50 GHz) and probing station. Probing by 100 µm-pitch GSG probes was done at the face-side GSG pads of D1 VM chip and back-side GSG pads of the D2 VL chip.
Locations of 12 ports in D1 via-middle chip. Ports 10, 11 and 12 are connected to Ports 3, 9 and 6 in D2 via-last chip (Fig. 5), respectively. They are indicated by an enclosed box.

Fig. 4 Locations of 12 ports in D1 via-middle chip.

Locations of 9 ports in D2 via-last chip.

Fig. 5 Locations of 9 ports in D2 via-last chip.

1) Correlation with measurement: Fig. 6 presents the correlation study of the self impedance at Port 11 in single D1 VM chip. Fairly good correlation between results by the proposed modelling approach and measurement is observed with percentage error less than 50%. The discrepancy is likely caused by fabrication process variation and some error inherited from the VNCAP equivalent circuit model.

Fig. 6 Self impedance at Port 11 in D1 VM chip with VNCAPs: our approach vs. measurement.

2) Effects of TSVs and VNCAPs on impedance: Based on the proposed modeling approach, the effects of TSVs and VNCAPs on PDN impedance are discussed. As shown in Fig. 7, the effect of via-middle TSVs on impedance in the D1 VM chip is generally not very significant. At low frequencies, it can be seen that the impedance is lower in the presence of TSVs. This is due to the increase in capacitance with the parallel connection of GSG TSVs. The effect of via-last TSVs on impedance in the D2 VL chip is also similar. In the presence of VNCAPs, it can be clearly seen that the PDN impedance reduces significantly over the whole frequency range.

Fig. 7 Effect of via-middle TSVs and VNCAPs on self impedance at Port 11 in D1 VM chip. Results are based on proposed modeling approach.

B. 7-chip stack

1) Correlation with measurement: On-wafer measurement of the 7-chip stack was conducted by probing the back-side GSG pads of the topmost D2 VL chip in the stack. Fig. 8 shows fairly good correlation between the proposed approach and measurement for self impedance at Port 9 of top D2 VL chip after stacking 7 chips. The percentage error is less than 40%. Note that this error is inevitable with consideration of the complexity of a 7-chip stack. The discrepancy can be due to fabrication process variation in individual chips and the changes in material properties with frequencies.

Fig. 8 Self impedance at Port 9 of top D2 VL chip with VNCAPs after stacking 7 chips: our approach vs. measurement.

2) Effect of chip stacking on impedance: To analyse the change in PDN impedance with stacking, different number and combination of stacked chips without VNCAPs are simulated using the proposed modeling approach and compared (see Fig. 9). For the case after a D3 chip (contains only TSVs) is stacked to the bottom of the D2 chip, it is shown that the self impedance at Port 9 of D2 chip reduces significantly at low frequencies. This is because of the increase in overall capacitance due to the parallel configuration of GSG TSVs in the D3 chip. With increasing number of D3 chips stacked below the D2 chip, the longer
stacked TSVs in parallel results in the reduction of the overall inductance. Hence, the impedance is reduced at higher frequencies. For the case after the D1 chip is connected to the bottom of the 6-chip stack, it can be seen that the impedance further reduces but increases at higher frequencies above 8 GHz. This is probably due to the effect of the larger D1 chip which has a larger capacitance and inductance compared to the D2 chip.

V. CONCLUSIONS

We have performed power integrity modeling, analysis and measurement of a 7-chip stack including on-chip power grid, TSVs and VNCAPs. The hybrid full-wave and circuit approach yields simulation results that are in good correlation with measurement. Results show that the effects of via-middle and via-last TSVs on PDN impedance are generally less significant for the single chip. It also shows that the VNCAPs are effective in reducing the PDN impedance. Hence, VNCAPs might be a good alternative to active on-chip decoupling capacitors in 3D ICs. For the analysis of the 7-chip stack, it is interesting to note that the self impedance at Port 9 of the top chip actually reduces after the stacking as compared to a single D2 VL chip. Results have shown that the stacked TSVs affect PDN impedance at higher frequencies while the on-chip power grid affects PDN impedance over the whole frequency range. Further investigation is needed to understand their interactions. In addition, position of the port might also play a role and is to be explored in the next work.

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